AP2002/2003

Synchronous PWM with VFC Controller (Preliminary)

■ Features

- Single or Dual Supply Application
- 0.8V ± 1.0% Ref.
- Proprietary virtual frequency control
- Fast transient response.
- Synchronous operation for high efficiency (95%)
- On-chip power good, OVP and enable functions (AP2002)
- Small size with minimum external components
- Soft Start (AP2003 Internal SS)
- Industrial temperature range
- Under Voltage Lockout function

■ Applications

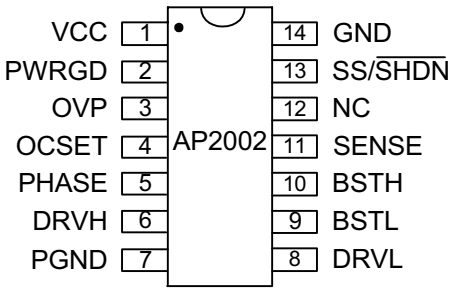
- Microprocessor core supply
- Low cost synchronous applications
- Voltage Regulator Modules (VRM)
- DDR termination supplies
- Networking power supplies
- Sequenced power supplies

■ General Description

The AP2002 is a low-cost, full featured, synchronous voltage-mode controller designed for use in single ended power supply applications where efficiency is of primary concern. Proprietary Virtual Frequency Control method provides the lowest number of external components and the smallest solution size without performance compromises. Synchronous operation allows for the elimination of heat sinks in many applications. The AP2002/2003 is ideal for implementing DC/DC converters needed to power advanced microprocessors in low cost systems, or in distributed power applications where efficiency is important. Internal level-shift, high-side drive circuitry, and preset shoot-thru control, allows the use of inexpensive N-channel power switches.
AP2002/2003 features include temperature compensated voltage reference, an internal 200Khz virtual frequency oscillator, undervoltage lockout protection, soft-start function (AP2003 internal SS) and current sense comparator circuitry. Power good signaling, shutdown, and over voltage protection are also provided AP2002.

■ Pin Assignments

(Top View)



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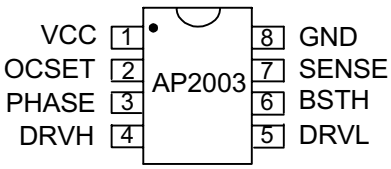
(Top View)



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■ Pin Descriptions

Name	Description
VCC	Chip supply voltage
PWRGD	Logic high indicates correct output voltage (open drain output)
OVP	Over voltage protection
OCSET	Sets the converter overcurrent trip point
PHASE	Input from the phase node between the MOSFETs
DRVH	High side driver output
PGND	Power ground
DRVL	Low side driver output
BSTL	Bootstrap, low side driver
BSTH	Bootstrap, high side driver
SENSE	Voltage sense input
NC	No Connection
SS/ $\overline{\text{SHDN}}$	Soft start, a capacitor to ground sets the slow start time
GND	Singal ground

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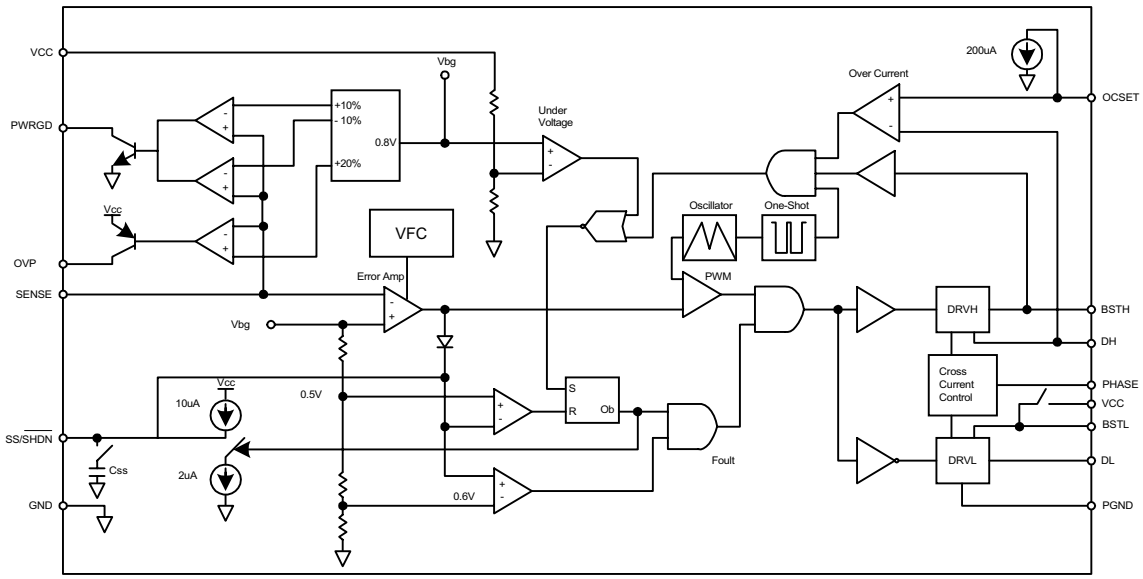
■ Ordering Information

AP 200 X X X

Part No.	Package	Packing
2 : AP2002 3 : AP2003	AP2002 S: SOP-14L AP2003 S: SOP-8L	Blank : Tube A : Taping

■ Block Diagram



■ Absolute Maximum Ratings

Symbol	Parameter		Max.	Unit
V_{IN}	VCC, BSTL to GND		-1 to 14	V
V_{PHASE}	PGND to GND		± 0.5	V
	PHASE to GND		-1 to 18	V
	BSTH to PHASE		14	V
Θ_{JC}	Thermal Resistance Junction to Case	AP2002	45	°C/W
		AP2003	60	
Θ_{JA}	Thermal Resistance Junction to Ambient	AP2002	115	°C/W
		AP2003	160	
T_{OP}	Operating Temperature Range		-40 to +85	°C
T_{ST}	Storage Temperature Range		-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering) 10 Sec.		300	°C

■ Electrical Characteristics

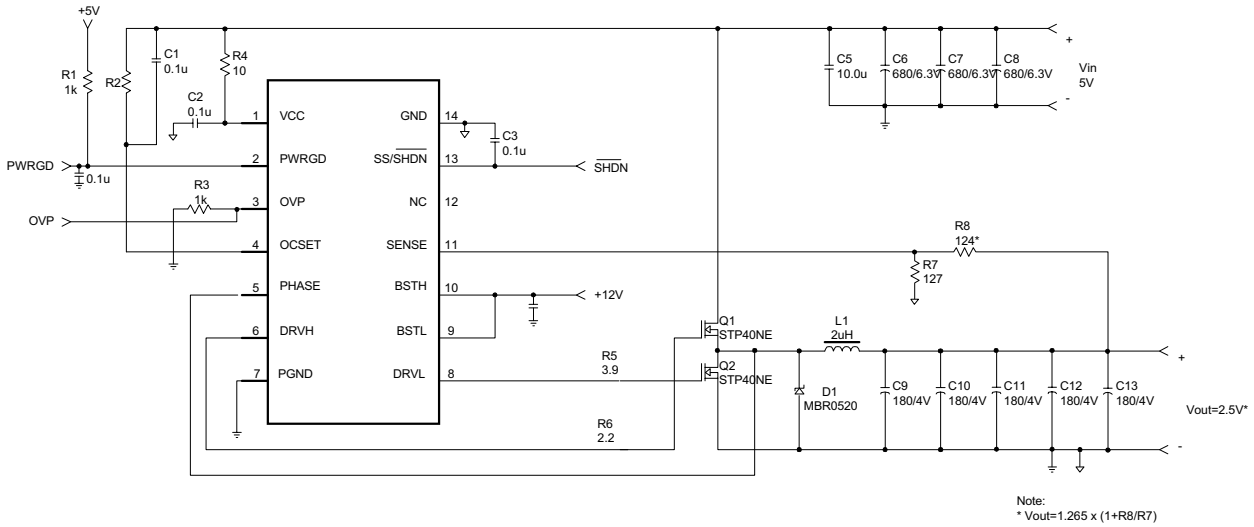
Unless specified: V_{CC} = 4.75V to 12.6V; GND = PGND = 0V; FB = V_O; V_{BSTL} = 12V; $V_{BSTH-PHASE}$ = 12V; T_J = 25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
V_{CC}	Supply Voltage	V_{CC}	4.2		12.6	V
I_{CC}	Supply Current	EN = V_{CC}		6	10	mA
ΔV_{LINE}	Line Regulation	VO = 2.5V		0.5		%
Error Amplifier						
A_{OL}	Gain (A_{OL})			50		dB
I_B	Input Bias			5	8	uA
Oscillator						
F_{OSC}	Oscillator Frequency		180	200	220	Khz
DC_{MAX}	Oscillator Max Duty Cycle		90	95		%
Mofset Drivers						
I_{DH}	DH Source/Sink	$V_{BSTH} - V_{DH}$ =4.5V $V_{DH} - V_{PHASE}$ = 2V	1			A
I_{DL}	DL Source/Sink	$V_{BSTH} - V_{DL}$ = 4.5V $V_{DL} - V_{PGND}$ = 2V	1			A
Protection						
D_{TH}	OVP Threshold Voltage			20		%
I_{OVP}	OVP Source Current	V_{OVP} = 3V	10			mA
D_{PG}	Power Good Threshold		88		112	%
T_{DEAD}	Dead Time		45		100	nS
I_{OCSET}	Over Current Set Isink	2.0V ≤ V_{OCSET} ≤ 12V	180	200	220	uA
Reference						
V_{REF}	Reference Voltage	0°C to 70°C	1.252	1.265	1.278	V
	Accuracy		-1		+ 1	%
Soft Start						
I_{SSC}	Charge Current	V_{SS} = 1.5V	8.0	10	12	uA
I_{SSD}	Discharge Current	V_{SS} = 1.5V	1.3	2	2.7	uA

Note 1. Specification refers to Typical Application Circuit.
Note 2. This device is ESD sensitive. Use of standard ESD handling precautions is required.

■ Typical Application Circuit

(1)



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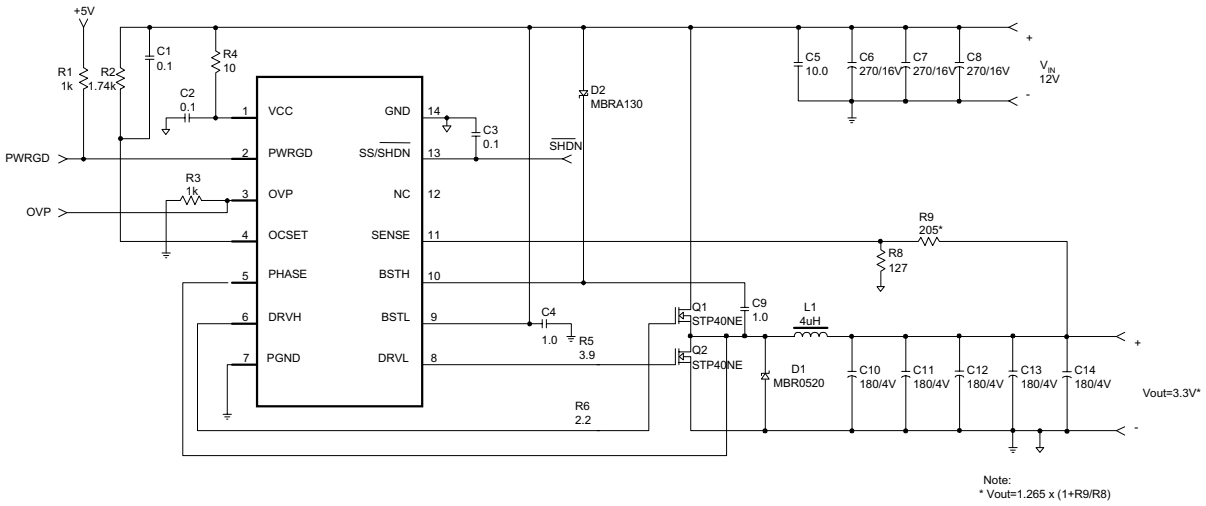


12V$_{IN}$ with Bootstrapped BSTH

■ Function Description

Synchronous Buck Converter

Primary V_{CORE} power is provided by a synchronous, voltage-mode pulse width modulated (PWM) controller. This section has all the features required to build a high efficiency synchronous buck converter, including "Power Good" flag, shut-down, and cycle-by-cycle current limit.

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier. The external resistive divider reference voltage is derived from an internal trimmed-bandgap voltage reference. The inverting input of the error amplifier receives its voltage from the SENSE pin.

The internal oscillator uses an on-chip capacitor and trimmed precision current sources to set the oscillation frequency to 200Khz. The triangular output of the oscillator sets the reference voltage at the inverting input of the comparator. Proprietary Virtual Frequency Control method provides the lowest number of external components and the smallest solution size without performance compromises. When the oscillator output voltage drops below the error amplifier output voltage, the comparator output goes high. This pulls DL low, turning off the low-side FET, and DH is pulled high, turning on the high-side FET (once the cross-current control allows it). When the oscillator voltage rises back above the error amplifier output voltage, the comparator output goes low. This pulls DH low, turning off the high-side FET, and DL is pulled high, turning on the low-side FET (once the cross-current control allows it).

As SENSE increases, the output voltage of the error amplifier decreases. This causes a reduction in the on-time of the high-side MOSFET connected to DH, hence lowering the output voltage.

Under Voltage Lockout

The under voltage lockout circuit of the AP2002/2003 assures that the high-side MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if V_{CC} falls below 4.1V. Normal operation resumes once V_{CC} rises above 4.2V.

Over-Voltage Protection

The over-voltage protection pin (OVP) is high only when the voltage at SENSE is 20% higher than the target value programmed by the external resistor divider. The OVP pin is internally connected to a PNP's collector.

Power Good

The power good function is to confirm that the regulator outputs are within +/- 10% of the programmed level. PWRGD remains high as long as this condition is met. PWRGD is connected to an internal open collector NPN transistor.

Soft Start

Initially, SS/$\overline{\text{SHDN}}$ sources 10uA of current to charge an external capacitor. The outputs of the error amplifiers are clamped to a voltage proportional to the voltage on SS/$\overline{\text{SHDN}}$. This limits the on-time of the high-side MOSFETs, thus leading to a controlled ramp-up of the output voltages. (AP2003 internal soft start function, time delay setting around 1mS.)

$R_{DS(ON)}$ Current Limiting

The current limit threshold is set by connecting an external resistor from the V_{CC} supply to OCSET. The voltage drop across this resistor is due to the 200uA internal sink sets the voltage at the pin. This voltage is compared to the voltage at the PHASE node. This comparison is made only when the high-side drive is high to avoid false current limit triggering due to uncontributing measurements from the MOSFETs off-voltage. When the voltage at PHASE is less than the voltage at OCSET, an overcurrent condition occurs and the soft start cycle is initiated. The synchronous switch turns off and SS/$\overline{\text{SHDN}}$ starts to sink 2uA. When SS/$\overline{\text{SHDN}}$ reaches 0.8V, it then starts to source 10uA and a new cycle begins.

■ Function Description (Continued)

Hiccup Mode

During power up, the SS/$\overline{SHDN}$ pin is internally pulled low until V_{CC} reaches the undervoltage lockout level of 4.2V. Once V_{CC} has reached 4.2V, the SS/$\overline{SHDN}$ pin is released and begins to source 10uA of current to the external soft-start capacitor. As the soft-start voltage rises, the output of the internal error amplifier is clamped to this voltage. When the error signal reaches the level of the internal triangular oscillator, which swings from 1V to 2V at a fixed frequency of 200Khz, switching occurs. As the error signal crosses over the oscillator signal, the duty cycle of the PWM signal continues to increase until the output comes into regulation. If an over-current condition has not occurred the soft-start voltage will continue to rise and level off at about 2.2V.

An over-current condition occurs when the high-side drive is turned on, but the PHASE node does not reach the voltage level set at the OCSET pin. The PHASE node is sampled only once per cycle during the vally of the triangular oscillator. Once an over-current occurs, the high-side drive is turned off and the low-side drive turns on and the SS/$\overline{SHDN}$ pin begins to sink 2uA. The soft-start voltage will begin to decrease as the 2uA of current discharge the external capacitor. When the soft-start voltage reaches 0.8V, the SS/$\overline{SHDN}$ pin will begin to source 10uA and begin to charge the extenal capacitor causing the soft-start voltage to rise again. Again, when the soft-start voltage reaches the level of the internal oscillator, switching will occur.

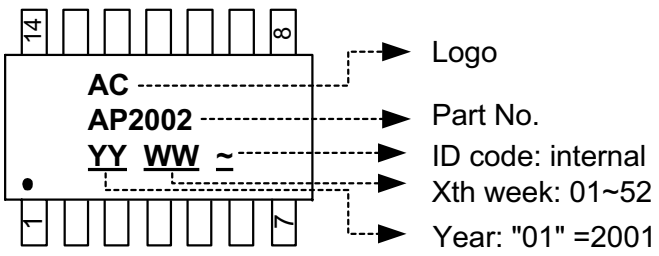
If the over-current condition is no longer present, normal operation will continue. If the over-current condition is still present, the SS/$\overline{SHDN}$ pin will again begin to sink 2uA. This cycle will continue indefinitely until the over-current condition is removed.

In conclusion, below is shown a typical “12V Application Circuit” which has a BSTH voltage derived by bootstrapping input voltage to the PHASE node through diode D1. This circuit is very useful in cases where only input power of 12V is available.

In order to prevent substrate glitching, a small-signal diode should be placed in close proximity to the chip with cathode connected to PHASE and anode connected to PGND.

■ Marking Information

(Top View)



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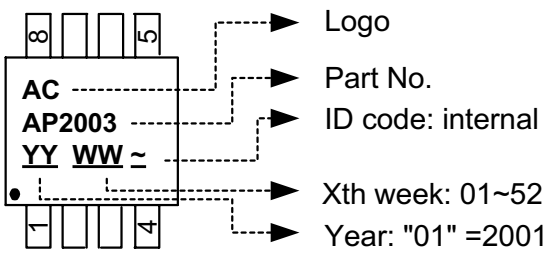
(Top View)



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■ Package Information

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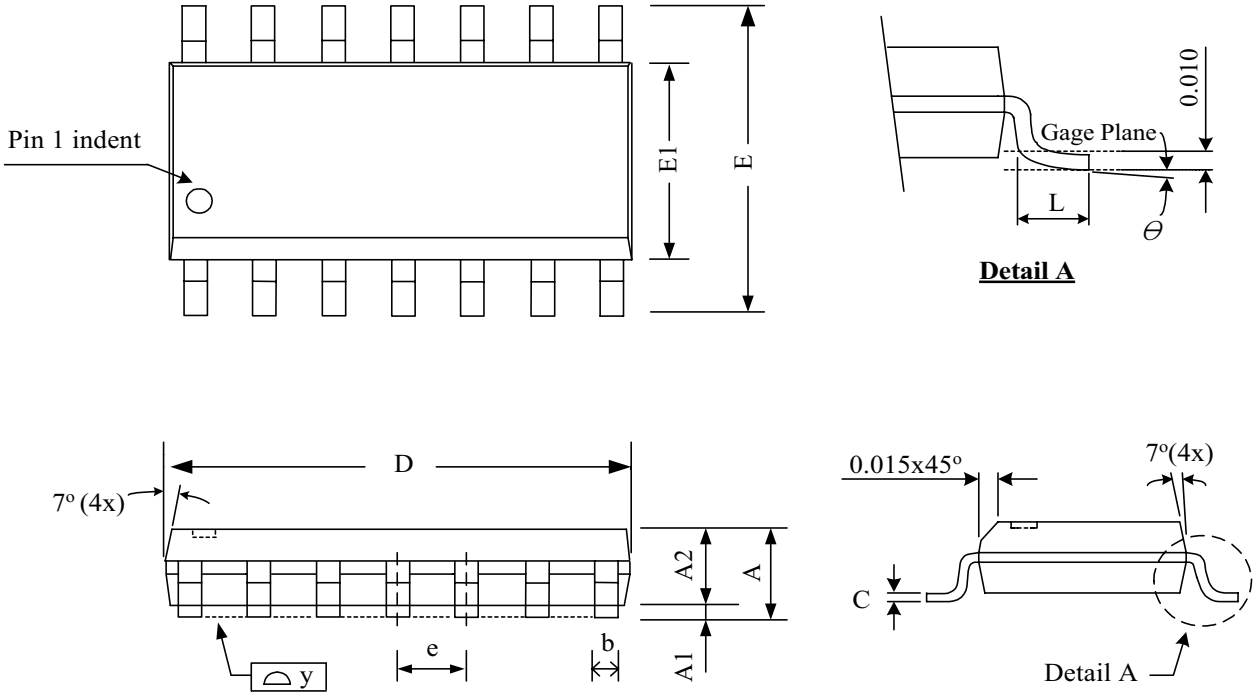
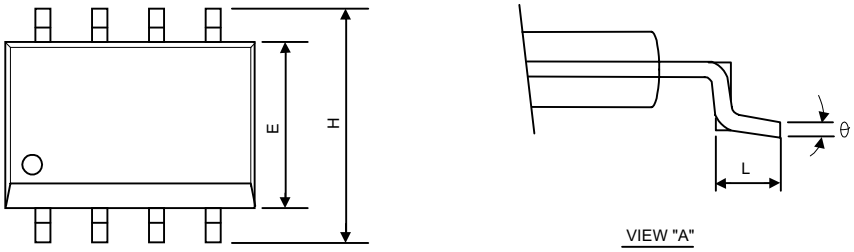
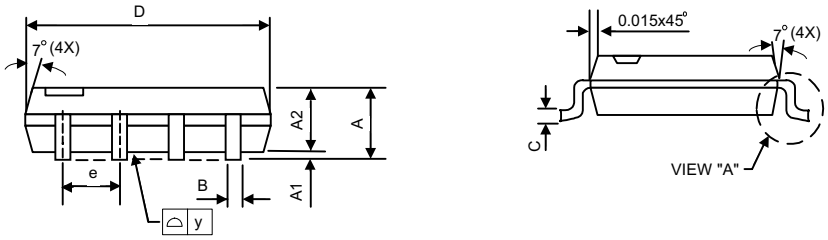


Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.47	1.60	1.730	0.0580	0.063	0.0680
A1	0.10	—	0.250	0.0040	—	0.0100
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.510	0.0130	0.016	0.0200
C	0.19	0.20	0.250	0.0075	0.008	0.0098
D	8.53	8.64	8.740	0.3360	0.340	0.3440
E	5.79	5.99	6.200	0.2280	0.236	0.2440
E1	3.81	3.91	3.990	0.1500	0.154	0.1570
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.270	0.0150	0.028	0.0500
Y	—	—	0.076	—	—	0.0030
θ	0°	—	8°	0°	—	8°

■ Package Information (Continued)

(2) Package Type: SOP-8L





Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.0550	0.063	0.069
A1	0.10	–	0.25	0.0400	–	0.100
A2	1.30	1.45	1.50	0.0510	0.057	0.059
B	0.33	0.41	0.51	0.0130	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	4.85	5.05	0.1890	0.191	0.199
E	3.80	3.91	4.00	0.1500	0.154	0.157
e	–	1.27	–	–	0.050	–
H	5.79	5.99	6.20	0.2280	0.236	0.244
L	0.38	0.71	1.27	0.0150	0.028	0.050
y	–	–	0.10	–	–	0.004
θ	0°	–	8°	0°	–	8°